RISCV-DSP
Digital Signal Processors

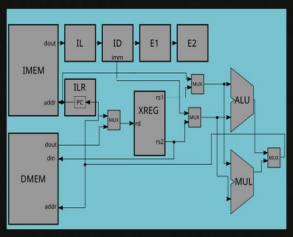
Brown Deer Technology

RISCV-DSP processing cores implement features and instruction set architecture extensions to create a family of DSPs targeting application-specific design requirements.

Bit Width	Standard					Extension			AI/Edge XPU
	E	I	M	F	D	Q	Z	X	
20-bit	✓					✓		✓	✓
24-bit	✓		✓	✓		✓		✓	✓
32-bit	✓	✓	✓	✓		✓	✓	✓	✓
64-bit		✓	✓	✓	✓		✓	✓	✓

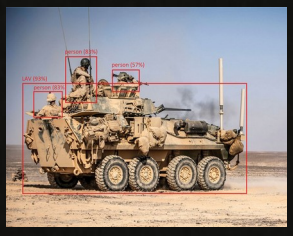
Processor Features

- Harvard architecture memory interface
- Embedded fixed-point operations (RV32Q)
- Native complex-valued operations (RV32Z)
- Extended execution coprocessor interface (RV32X)
- Variable bit-width core architecture (RV20/RV24)



Available Technology

- RISC-V DSP cores are available for use and licensing
- Open-hardware reference designs available in Verilog HDL
- Compiled devices available for emulation and FPGA integration
- Fully integrated into the COPRTHR® toolchain as a device library



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